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TITLE: Microprocessor having an on-chip CPU fetching a debugging routine from a memory in an external debugging device in response to a control signal received through a debugging port

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INVENTOR-INFORMATION:

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US-CL-CURRENT: 710/5, 710/71 , 712/227 , 714/30 , 714/34 , 714/35

ABSTRACT:

There is disclosed a computer system including a microprocessor on an **integrated circuit** chip comprising an on-chip CPU and a **debugging** port connected to a communication bus on the **integrated circuit** and to an external **debugging** computer device. The external **debugging** device is operable to transmit control signals through the **debugging** port: a) to stop execution by the CPU of instructions obtained from a first on-chip memory; b) to provide from a second memory associated with the external **debugging** computer device a **debugging** routine to be executed by the CPU; and c) to restart operation of the CPU after the routine with execution of instructions from an address determined by the external **debugging** device. The on-chip CPU is operable with code in the first memory which is independent of the **debugging** routine. A method of operating such a computer system with an external **debugging** device is also disclosed.

21 Claims, 17 Drawing figures

Exemplary Claim Number: 1

Number of Drawing Sheets: 10

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Abstract Text - ABTX (1):

There is disclosed a computer system including a microprocessor on an **integrated circuit** chip comprising an on-chip CPU and a **debugging** port connected to a communication bus on the **integrated circuit** and to an external **debugging** computer device. The external **debugging** device is operable to transmit control signals through the **debugging** port: a) to stop execution by the CPU of instructions obtained from a first on-chip memory; b) to provide from a second memory associated with the external **debugging** computer device a **debugging** routine to be executed by the CPU; and c) to restart operation of the CPU after the routine with execution of instructions from an address determined by the external **debugging** device. The on-chip CPU is operable with code in the first memory which is independent of the **debugging** routine. A method of operating such a computer system with an external **debugging** device is also

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disclosed.

Brief Summary Text - BSTX (7):
The invention provides a computer system including a microprocessor on an integrated circuit chip comprising an on-chip CPU with a plurality of registers and a communication **bus** providing a parallel communication path between said CPU and a first memory local to said CPU, said integrated circuit device further comprising a debugging port connected to said **bus** on the integrated circuit chip and to an external debugging computer device having a second memory, said external debugging device being operable to transmit control signals through said debugging port (a) to **stop** execution by the CPU of instructions obtained from said first memory (b) to provide from said second memory a debugging routine to be executed by the CPU and (c) to restart operation of the CPU after said routine with execution of instructions from an address determined by said external debugging device, whereby said on-chip CPU is operable with code in said first memory which is independent of said debugging routine.

Brief Summary Text - BSTX (11):
The invention includes a method of debugging a computer system which comprises a microprocessor on an integrated circuit chip with an on-chip CPU, a plurality of registers and a communication **bus** providing a parallel communication path between said CPU and a first memory local to said CPU, said integrated circuit device having a debugging port connected to said **bus** and to an external debugging computer device having a second memory, said method comprising transmitting control signals from said external debugging device through said debugging port (a) **stopping** execution by the CPU of instructions obtained from said first memory (b) executing by the CPU a debugging routine provided from said second memory and (c) restarting operation of the CPU after said debugging routine with execution of instructions from an address determined by said external debugging device, whereby said on-chip CPU is operated with code in said first memory which is independent of said debugging routine.

Claims Text - CLTX (1):
1. A computer system including a microprocessor on an integrated circuit chip comprising an on-chip CPU with a plurality of registers and a communication **bus** providing a parallel communication path between said CPU and a first memory local to said CPU, said first memory storing instructions for operation of said CPU, said integrated circuit device further comprising a debugging port connected to said **bus** on the integrated circuit chip and to an external debugging computer device having a second memory, said chip having circuitry responsive to first, second and third control signals from said external debugging device via said debugging port whereby said first control signal **stops** execution by the CPU of instructions obtained from said first memory, said second control signal causes said CPU to fetch from said second memory a debugging routine to be executed by the CPU and said third control signal restarts operation of the CPU after said debugging routine with execution of instructions from an address determined by said external debugging device, whereby said instructions in said first memory are independent of said debugging routine.

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Current US Cross Reference Classification - CCXR (4):
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Current US Cross Reference Classification - CCXR (5):